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Compro's RSX

White Paper

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List of Acronyms and Abbreviations

Abbreviation	Definition
ASIC	Application-Specific Integrated Circuit
CMOS	Complementary Metal-Oxide-Semiconductor
CONCEPT/32	Model or class of the computer
CPU	Central Processing Unit
DMC	Direct Mapped Cache
DRAM	Dynamic Random Access Memory
HSD	High Speed Device
I/O	Input/Output
IEEE	Institute of Electrical and Electronics Engineers
MB	Mega Byte
MHSD	Memory Mapped HSD™
PC	Personal Computer
POSIX®	Portable Operating System Interface
RISC (processor)	Reduced Instruction Set Computer
RMS	Reflective Memory System
RSX II	Class of Encore computer
SCSI	Small Computer System Interface
SRAM	Static Random Access Memory
TCP/IP	Transmission Control Protocol / Internet Protocol
VME	Versa Module Eurocard

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1 Overview

Compro's RSX II computer is a Reduced Instruction Set Computer (RISC) processor with dual high-performance modes of operation, RISC and CONCEPT/32 compatibility. Innovations such as large multi-ported Direct Mapped Cache (DMC), separate real-time Input/Output (I/O) bus, and state-of-the-art RISC technology enhance Compro's proven real-time capabilities. RSX II serves as a perfect 'bridge' enabling Compro CONCEPT/32 users to move to the price/performance advantages of RISC technology without requiring any changes to current software.

2 Features

- RISC Processor
- New Small Computer System Interface (SCSI) Subsystem
- Large Cache Memory Design (Purchased Separately)
- Industry Standards
- Separate Real-time I/O Bus
- Multiprocessor Design
- Special Real-Time Features
- CONCEPT/32® Compatibility Mode

3 RISC Processor

The Compro RSX II computer is a RISC processor with dual operating modes. In native RISC mode, it provides a high-performance state-of-the-art RISC architecture designed for the most demanding real-time applications. In CONCEPT/32 compatibility mode, the RSX II can execute any CONCEPT/32 object code. RSX II systems can simultaneously execute tasks in both modes. Tools are provided to easily move object code from compatibility mode to native RISC mode.

The RSX II processor is a highly pipelined RISC design, which requires only one Central Processing Unit (CPU) execution cycle for most instructions. It achieves much of its speed from multiple independent functional units capable of operating in parallel during multi-cycle instructions (Figure 1). This is implemented using 1 micron CMOS chip technology and a complement of cell-based and semi-custom Application Specific Integrated Circuits (ASIC) to create the dual mode environments. The dual independent 64-bit data paths (128 bits total) to memory and highly paralleled RISC design yield a system capable of achieving one cycle per instruction execution. Dual, independent 28-bit address paths (56 bits total) are provided between the processor and memory. The Execution Unit and the Instruction Unit each have access to both the data and address paths. The parallel execution of integer and floating point operations contribute to this high execution rate. Innovative superscalar floating point can

initiate two floating point operations in one CPU cycle, thus making the system ideally suited for demanding scientific environments.

The local memory bus provides a private path between the processor and memory system. Its 213 MB per second bandwidth easily sustains the high processing rates of the RISC mode. It is complemented by an independent real-time I/O bus that does not interfere with the CPU access to memory. The memory system is quad-ported to achieve parallel throughput of real-time I/O streams into memory without stealing any cycles from the CPU. One of the four memory ports is utilized by Compro's Reflective Memory System (RMS) that permits connectivity of multiple systems.

Floating point architecture is one of RSX II's more innovative attributes. It is built upon a multiply-accumulate function that executes two floating point operations in one instruction. Among these instruction pairs are multiply-add, multiply-subtract, divide-add, divide-subtract and others. This results in extremely high processing rates for floating point intensive applications such as many forms of simulation. Also, certain mathematical sequences such as polynomial evaluation (cumulative multiply-add sequences) are accelerated. RSX II boasts of one to two microsecond intrinsic (SINE, COSINE, etc.) due to these powerful floating point features.

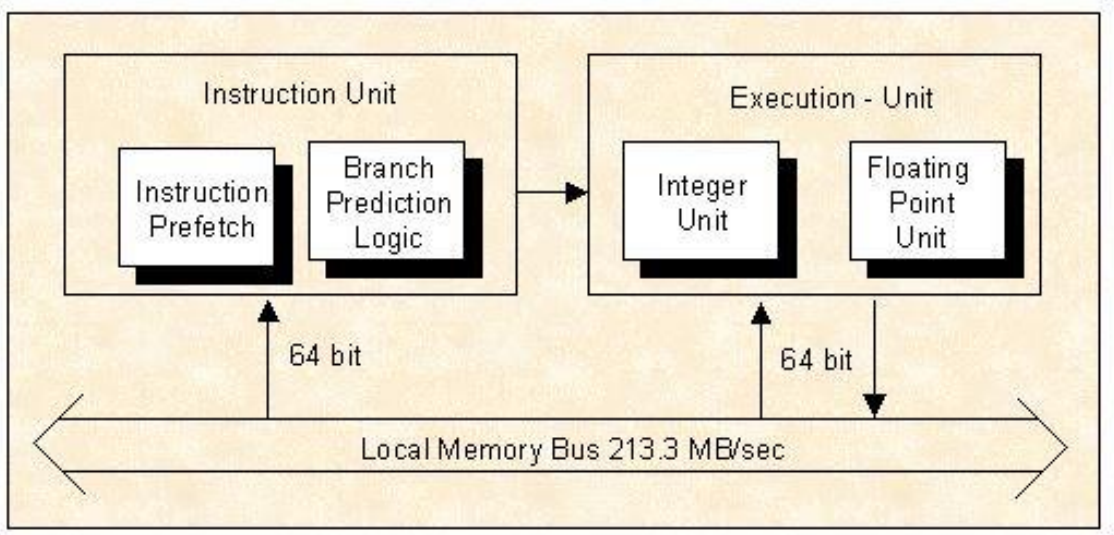

Figure 1. Parallel Options

4 Large Cache Memory Design

(Purchased Separately)

Influenced largely by Compro's long experience in real-time, the RSX II memory system features a very large DMC design. Starting at 4 MB, the DMC delivers unprecedented user cache-management and control. First, the cache is expandable up to a total of 16 MB. Second, the cache is programmable with tools that enable you to select which portions of which tasks are to reside in cache and which are not. The main memory is configurable up to 256 MB of dynamic RAM (DRAM), minus the amount of DMC in the System. The DMC is implemented with very fast static RAM (SRAM).

The direct mapped design permits a simplified model for multi-CPU cache coherency and non-intrusive real time I/O. The DMC is quad-ported and operates at an aggregate rate of over 290 MB per second across all ports. Two ports are for the CPU, one port is for the real-time I/O bus, and one port is for RMS. Any updates to the DMC occur in one cycle whether from the RMS port, I/O port, or CPU. This permits very deterministic system design of multiple computers with simultaneous I/O without impacting CPU performance.

By making the DMC the master interface for all memory access, cache coherency is ensured. All CPU references to main memory filter through the DMC (Figure 2). If the CPU requests data from addresses outside those in the DMC, the DMC issues the requests to main memory. Direct mapping into contiguous address ranges eliminates the need for cache flushing and duplication of cache addresses with main memory addresses. The CPU views DMC memory as main memory and there are no 'cache write-throughs' (except for RMS which does 'reflect' memory writes across the RMS bus). Compro's RSX II operating systems include software tools that enable you to distribute portions of tasks between DMC addresses and main memory addresses. In real-time environments, this provides optimum user control. Regardless of simultaneous 1/0 traffic or multiprocessor load, RSX II delivers performance to an unprecedented degree for RISC systems. Cache 'miss' and 'flush' problems are virtually eliminated.

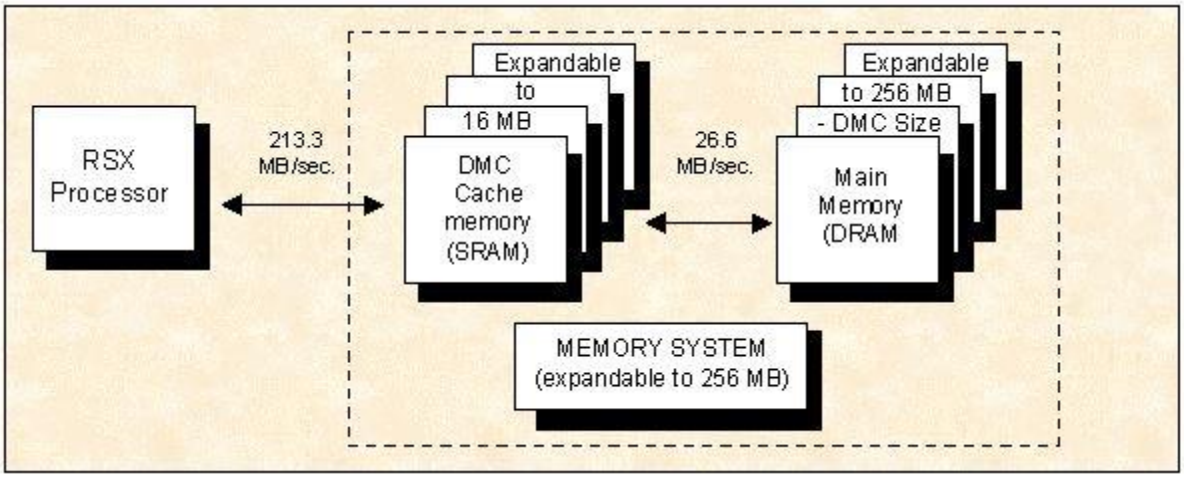

Figure 2. CPU/Cache/Memory System Design

5 Industry Standards

Compro RSX II exemplifies Compro's continuing commitment to industry standards. It features:

- IEEE-754 floating point for data sharing with other RISC systems
- Ethernet and associated protocols such as TCP/IP
- High performance Versa Module Eurocard (VME) bus option
- Standard SCSI ports and asynchronous ports
- Additional standards available through the compatible Compro 90 Family

There are a host of languages that track industry standards such as Ada . FORTRAN, and C. All Compro systems are committed to full Portable Operating System Interface (POSIX®) compliance and Compro RSX II is no exception.

6 Separate Real-Time I/O Bus

The separation of the real-time I/O bus to the DMC provides over 26 MB of pure I/O throughput (Figure 3). To take advantage of this high bandwidth, a collection of real-time interfaces such as the Memory Mapped HSD™ (MHSD) are available. The MHSD can sustain I/O at 13 MB per second and multiple MHSDs can connect to the bus. High-performance VME transfers, disk transfers and other I/O traffic can be active simultaneously.

The RSX II real-time I/O bus is based on Compro's pre-emptible SeIBUS™ , which can interleave prioritized packets of smaller transfers among larger transfers. This means there is no real performance penalty due to larger transfers 'hogging' the bus for an entire transmission. Smaller real-time bursts can always interleave with the larger transfers. This type of I/O available on RSX II is atypical of most RISC systems and more typical of mainframe-style channel I/O.

The entire above-mentioned activity can occur without significantly impacting CPU performance. In fact, all 26 MB of I/O bandwidth can be saturated without significantly slowing down the CPU due to the very high aggregate throughput of the multi-ported DMC.

An additional I/O capability is realized when using the RMS port into the DMC as an I/O channel. Over 53 MB per second of I/O is available through RMS to supplement the 26 MB of real-time I/O through the real-time I/O bus. This gives an aggregate of over 79 MB of I/O into the DMC without cache coherency problems and without significantly impacting CPU performance.

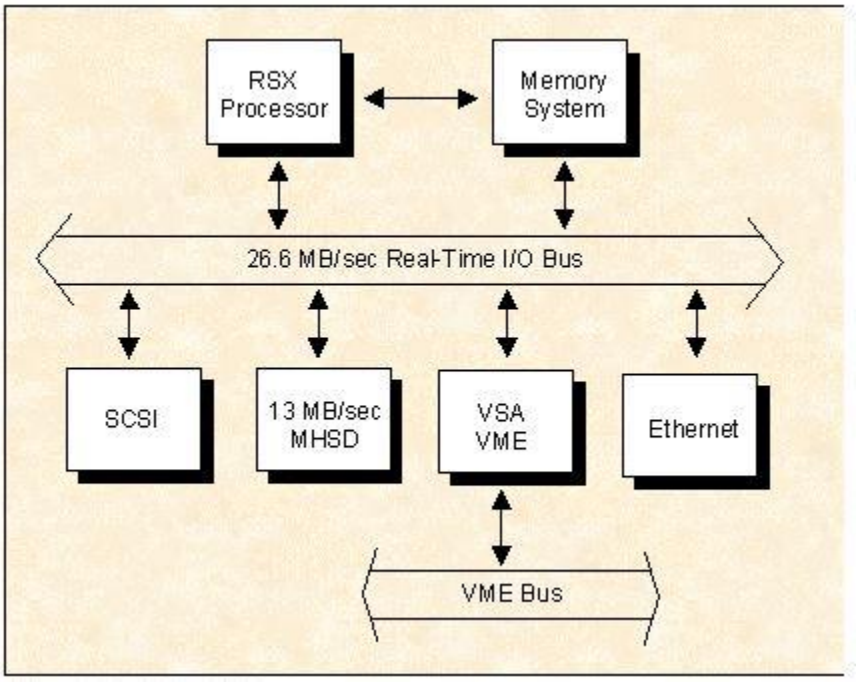

Figure 3. Real-Time I/O Bus

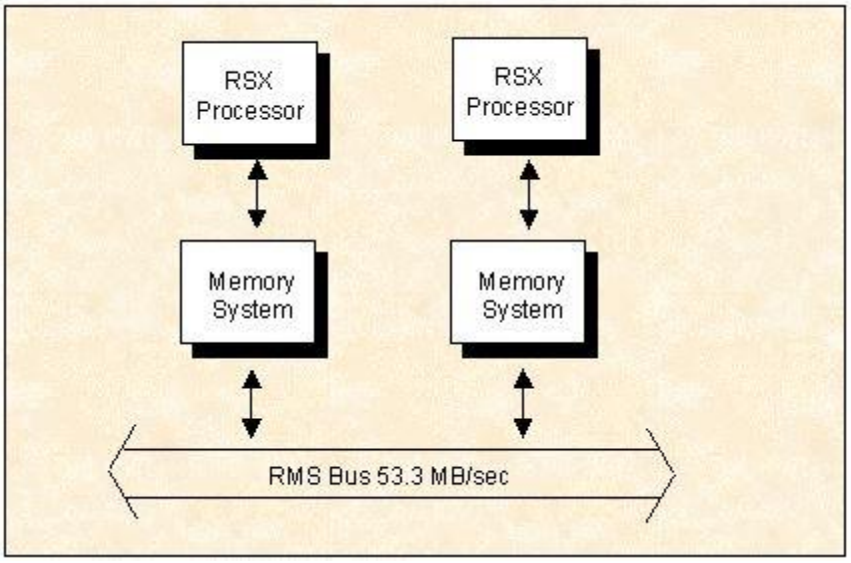

Figure 4. Integrated Multi-CPU Cache Coherency

7 Multi-Processor Design

RSX II systems are designed for integration of multiple processors into one total system. The key technology for the integration is Compro's award winning patented RMS. Since RSX II connects to RMS via the DMC cache coherency is ensured (Figure 4). Updates to global memory from other CPUs are immediately seen in all CPUs with minimal latency and no cache 'flushing' penalties in any CPU.

For CONCEPT/32 users. RSX II CPUs can be installed in existing SelCONNECTION™ cabinets to provide easy upgrades from MULTISel™ to RSX II RISC systems.

8 Special Real-Time Features

In addition to hardware architecture features such as RISC, large cache, and real-time I/O, RSX II software is optimized for real-time. The real-time kernel is built for very fast context switch, interrupt response time, task suspend/resume, and minimal interrupt blockout producing the best real-time performance in the industry. Users can bypass almost any operating system overhead to directly attach to interrupts and easily implement special device handlers.

User tasks have access to eight externally connected traps. These external traps require less than five-microsecond latency to get to the first instruction in the trap handler. Each of the external trap lines has a dedicated memory location associated with it. This dedicated memory location stores the starting address of the trap service routine for that particular trap. The priorities associated with these external traps are higher than external interrupts, but lower than system integrity for traps.

The CPU includes eight internal timers that can be used by both the operating system and the user's tasks and offers a range of resolutions up to 75 nanoseconds. One interval timer is privileged (for operating system use) and can be stopped, started, loaded, and examined. This programmable 32-bit interval timer can be used to generate interrupts at prescribed intervals from 150 nanoseconds and up. The other interval timers have extended features to act as privileged I/O interrupting timers or as non-interrupt unprivileged register access timers.

A clock-calendar function provides modifiable date and time-of-day with seconds resolution and continues to run when the system is powered off.

9 CONCEPT/32 Compatibility Mode

Compro RSX II can execute any standard MPX-32 object code in compatibility mode. The dual mode design permits MPX-32 operating system images and load modules to port directly to RSX II without recompilation or relinking. Both base and non-base instruction sets are supported. All CONCEPT/32 data types including CONCEPT/32 floating point format are supported. CONCEPT/32 SeIBUS devices are supported. Virtually all software and hardware that can run on an MPX-32 3.X system are supported. Older versions of hardware and MPX-32 software can be upgraded to RSX II compatibility mode. See the Compro Site Audit or your Compro representative for more Information about upgrading pre-MPX-32 3.X systems.

There are many native mode features that can be used. Over time, after moving applications to RSX II compatibility mode including expanded logical address space. Demand paging, IEEE-754 floating point, directly vectored SVCs, and more. RSX II makes it possible to transition to as few or as many of these native mode features as desired. If compatibility mode is sufficient for some tasks, they need not be changed. As the applications demand or on an as-needed basis, some tasks can begin to take advantage of native mode features while other tasks are running in compatibility mode. This convenience eliminates the high cost of conversion and eases the transition of applications to the features and benefits of RSX II RISC technologies.

10 Model Numbers

10.1 4841D

The RSX II System is supplied with the host node cabinet, chassis with 8/0 backplane, 4-slot SCSI chassis, RSX II processor board, multi-funtion processor, and new SCSI subsystem. DMC and memory are purchased separately, see below for model numbers.

Prerequisite: 1965-PC-System#

Corequisite: DMC and 4 or 16 MB SRAM

10.2 4844C

The RSX II Expansion Node includes chassis with 8/0 backplane, RSX II processor board, and RMS port to DMC. DMC and memory are purchased separately, see below for model numbers.

Prerequisite: 4841D or 4844A

Corequisite: DMC and 4 or 16 MB SRAM

10.3 4844A

The RSX II Node system, 4844A, includes the Expansion Node (above) and host node cabinet.

Prerequisite: 1965-PC-System (not required if being used to expand existing 6841 system)

Corequisite: DMC and 4 or 16 MB SRAM

10.4 4633-(0/1/2/3/4)(0/1/2)

The RSX II upgrade package includes the RSX II processor board, CMOS CPU credit, Memory credit, and site audit. DMC and memory are purchased separately, see below.

Prerequisite: 1965-PC System (if being used as host).

Co-requisite: DMC and 4 or 16 MB SRAM

Suffix Modifier: 4633-ab

a	=	0	Upgrade from 32/6744 Cabinets (MULTISel products)
	=	1	Upgrade from 32/67 71-inch Cabinets
	=	2	Upgrade from 32/6742 Cabinets (SelPAC 32-inch wide cabinets)
	=	3	Upgrade from 32/6744 Cabinets (Tall MULTISel cabinets)
	=	4	Upgrade from 32/6741 Cabinets (SelPAC 22-inch wide cabinets)
b	=	0	Initial CPU
	=	1	Add-on CPU
	=	2	Mixed CPU (one each 32/67 or SMOS CPU and one Compro RSX CPU)

10.5 Memory Options (Remanufactured)

- R3030-0(0/1/2/3/4/5) - 4 MB SRAM, 75 ns
- R3031-0(0/1/2/3/4/5) - 16 MB SRAM, 75 ns
